Online Faculty Development Programme on

Foundations of VLSI Design Verification

23rd June – 6th July 2025

Jointly organized by Electronics and ICT Academies
Established by the Ministry of Electronics and Information Technology, Govt. of India

IIITDM Jabalpur | IIT Guwahati | IIT Kanpur | IIT Roorkee | MNIT Jaipur | NIT Patna | NIT Warangal

Objective (Electronics & ICT Academy-Phase II)

1. To conduct specialized FDPs for faculty/mentor training in line with the vision of MeitY by promoting emerging areas of technology and other high-priority areas that are pillars of both the "Make in India" and the "Digital India" programs.
2. To promote synergy and collaboration with industry, academia, universities and other institutions of learning, especially in emerging technology areas.
3. To support the National Policy on Electronics 2019 (NPE 2019) which envisions positioning India as a global hub for ESDM sector, including MeitY Schemes/policies such as Programme for Semiconductors and Display Fab Ecosystem; India AI; National Programme on AI, Production Linked Incentive Scheme for IT Hardware & Large-Scale Electronics Manufacturing; EMC; SPECS; Chips to System (C2S); etc.
4. To promote standardization of FDPs through Joint Faculty Development Programmes.
5. To support the vision of the National Education Policy (NEP 2020), which mandates that Indian educators go through at least 50 hours in professional development programmes per year.
6. To design, develop & deliver specialized FDPs on emerging technologies/ niche areas/ specialized modules for specific research areas for Faculty in Higher Education Institutions (HEI), besides FDPs on multi-disciplinary areas connected with ICT tools and technologies and other digital hybrid domains, covering a wide spectrum of Engineering. and non-engineering colleges, polytechnics, ITIs, and PGT educators.

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An intensive 40 hours Training Programme will be offered in online mode and is intended for faculty and doctoral students of engineering and technological institutions. The training program will explore the theme of Foundations of VLSI Design Verification which is a skill in high demand in the VLSI/semiconductor industry. The classes will be held during **7 - 9 PM (workdays) and 5 hours each on Saturday and Sunday.**

Programme Modules:

- Introduction to Design Verification
- Functional Simulation as a Verification Tool
- Testbench Development
- Sequential Circuit Verification
- Verilog Testbench Concepts
- Introduction to SystemVerilog as a Hardware Verification Language (HVL)
- Object-Oriented Programming in SystemVerilog
- Advanced Verification Techniques
- Comprehensive System Verification Example
- Industry Practices and Career Insights

Methodology:

- Lectures: Conceptual understanding and theoretical foundations
- Hands-on Labs: Practical application through guided exercises
- Mini Project: Integration of learned concepts in a comprehensive verification task
- Course materials will be provided during the course.

Prerequisites:

- Basic knowledge of digital design principles
- Familiarity with Verilog is beneficial but not mandatory

Registration Link: https://forms.gle/2eCCSja8LFF53ore9

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SCAN & PAY
UPI ID : iiitdmj@indianbk

Certification Fee: Academic (Faculty/Students): ₹ 500/-
Industry Professionals/Others: ₹ 1500/-
The fee covers course material and certification charges.

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